AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/584,566 Filing Date: May 31, 2000

Title: HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES

REMARKS

Claims 1-2, 7, 10-14, 16-17, and 19, are amended; claims 15 and 18, are cancelled, with prejudice; and claims 70-82 are added. As a result, claims 1-14, 16-17, 19-23, and 70-82 are now pending in this application.

§112 Rejection of the Claims

Claims 1-23 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. Applicants have made the necessary claim amendments, which are noted above, to address the Examiner's indefinite rejections with respect to independent claims 1, 7, and 14. Accordingly, these § 112 rejections are no longer appropriate.

§103 Rejection of the Claims

Claims 1-11, 13-17, and 19-23 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi et al. ("A Direct Tunneling Memory..."). In order to sustain an obviousness rejection, each and every element in the rejected claim must be taught or suggested in the cited references. Here, Horiguchi does not teach of disclose the structure recited in Applicants' amended independent claims 1, 7, and 14. Therefore, the rejections with respect to Horiguchi are no longer sustainable.

More specifically, Horiguchi does not teach a horizontal gate or horizontal control gate that is coupled to two opposing and parallel vertical gates or vertical control gates. Horiguchi, Figs. 1, 2, and 4. Applicants' novel structure of amended independent claims 1, 7, and 14 does include the horizontal gate or horizontal control gate coupled to two opposing and parallel vertical gates or vertical control gates.

This novel structure permits the total capacitance of memory devices to be about the same as that for conventional structures. However, unlike conventional structures, Applicants' novel structure simultaneously permits the floating gate capacitance to be much smaller than the control gate capacitances such that the majority of any voltage applied to the control gates will appear across the floating gate thin tunnel oxide. Thus, the devices having structures of Applicants' amended independent claims 1, 7, and 14 can be programmed by tunneling of

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/584,566 Filing Date: May 31, 2000

Title: HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES

electrons to and from the silicon substrate at lower control gate voltages than is possible in Horiguchi or conventional structures.

Claims 1-23 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi et al. in view of Watanabe (U.S. Patent No. 6,133,601) or Hong et al. (U.S. Patent No. 5,625,213). Again, each of the rejected claim elements must be taught or suggested in the cited references in order to sustain an obviousness rejection.

Watanabe does not teach or suggest any horizontal control gate or horizontal gate at all, and includes only two vertical gates there is no mention of a third, such that all three vertical gates are parallel to one another where at least two of the vertical gates are on opposite sides of the remaining vertical gate. To modify Watanabe to achieve the same would render the structures in Watanabe ineffective for their stated teaches and purposes. Correspondingly, Watanabe cannot be combined with Horiguchi or Hong to produce Applicants' amended independent claims 1, 7, and 14.

Hong teaches a single horizontal floating gate and horizontal control gate, and does not teach or disclose three vertical gates that are parallel to one another having at least two of those vertical gates connected at top portions to a horizontal gate, where the remaining vertical gate is not coupled to the horizontal gate or the other two vertical gates.

Moreover, Horiguchi cannot be modified with Hong, since Hong is directed to suppressing floating gate leakage where the floating gate and the opposing control gates are separated by control gate oxide for the control gates and structurally in alignment with the control gates. Thus, if Horiguchi were modified with Hong, the result would be a structure where the floating gate is coupled to any added horizontal control gate, and this would not permit Hong to achieve its stated purpose of avoiding floating gate leakage. Additionally, Applicants' amended claim 14 can include a control gate in the position listed in Horiguchi as a floating gate; this cannot be achieved with any combination of Horiguchi, Watanabe, and/or Hong.

Accordingly, none of the references, standing alone, or in various combinations with one another teach or suggest each and every element of Applicants' amended independent claims.

Thus, these rejections should be withdrawn.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/584,566 Filing Date: May 31, 2000

Title: HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

 $SCHWEGMAN, \, LUNDBERG, \, WOESSNER \, \& \, KLUTH, \, P.A.$

P.O. Box 2938

Minneapolis, MN 55402

612-349-9587

Date 20) (mg 107)

Timothy B. Clise

Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 20th day of June, 2003.

Name

Signature